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10/720,484	11/25/2003	Byoung-Chan Kim	053933-5058	4365

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MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
WILLIAMS, ALEXANDER O	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,484	KIM ET AL	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *9-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/720484 Attorney's Docket #: 053933-5058
Filing Date: 11/25/2003; claimed foreign priority to 9/4/2003

Applicant: Kim et al.

Examiner: Alexander Williams

Applicant's Amendment filed 2/2/2005 for the election of Group I (claims 1 to 8), filed 8/27/2004, has been acknowledged.

This application contains claims 9 to 11 drawn to an invention non-elected without traverse.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 3 to 5 to 7 are rejected under 35 U.S.C. § 102(e) as being anticipated by Corisis et al. (U.S. Patent Application Publication # 2003/0189256 A1).

1. Corisis et al. (figures 1 to 13) specifically figures 3 and 8 show a ball grid array (BGA) package **50** having a semiconductor chip **20a',20b'** with edge-bonding metal patterns **(45, see figure 1)** formed thereon, comprising: a substrate **52** having circuit patterns for electric connection formed therein (inherit); a center-bonding type semiconductor chip **20a',20b'** attached to the substrate, the semiconductor chip having center-bonding pads **(34, see figure 1)** formed on one side thereof; edge-bonding metal patterns **(45, see figure 1)** electrically connected to the center-bonding pads of the semiconductor chip, the edge bonding metal patterns being extended towards the edge regions of the center-bonding type semiconductor chip; connection members **56** for electrically connecting the edge bonding metal patterns extended towards the edge regions of the semiconductor chip to the circuit patterns of the substrate, respectively; a sealing material **58** for molding the substrate to protect the semiconductor chip; and solder balls **(shown at the bottom of 52)** attached to solder pads **(not shown, but inherit)** electrically connected to the circuit patterns of the substrate, respectively, for transmitting electric signals from the semiconductor chip to an external substrate, wherein the edge-bonding metal patterns **(45, see figure 1)** are in contact with both of the center-bonding pads **34** and the connection members **56**.

2. Corisis et al. (figures 1 to 13) specifically figure 8 show a ball grid array (BGA) package **50** having semiconductor chips **20a',20b'** with edge-bonding metal patterns **(45, see figure 1)** formed thereon, comprising: a substrate **52** having circuit patterns for electric connection formed therein; a first center-bonding type semiconductor chip **20a'** attached to the substrate, the first semiconductor chip having center bonding pads **(34, see figure 1)** formed on one side thereof; edge-bonding metal patterns **(45, see figure 1)** electrically connected to the

center-bonding pads of the first semiconductor chip, the edge-bonding metal patterns being extended towards the edge regions of the first center-bonding type semiconductor chip; a bonding member (**49, see figure 5**) applied to the first semiconductor chip to form a stacked structure; a second center-bonding type semiconductor chip **20b'** stacked on the first semiconductor chip via the bonding member, the second semiconductor chip having center-bonding pads (**34, see figure 1**) formed on one side thereof; edge-bonding metal patterns (**45, see figure 1**) electrically connected to the center-bonding pads of the second semiconductor chip, the edge-bonding metal patterns being extended towards the edge regions of the second center-bonding type semiconductor chip; connection members **56** for electrically connecting the edge bonding metal patterns of the first and second semiconductor chips to the circuit patterns (**inherit**) of the substrate, respectively; a sealing material **58** for molding the substrate to protect the first and second semiconductor chips; and solder balls (**shown on the bottom of 52**) attached to solder pads (**inherit**) electrically connected to the circuit patterns of the substrate, respectively, for transmitting electric signals from the first and second semiconductor chips to an external substrate wherein the edge-bonding metal patterns (**45, see figure 1**) are in contact with both of the center-bonding pads **34** and the connection members **56**, wherein the edge-bonding metal patterns (**45, see figure 1**) are in contact with both of the center-bonding pads **34** and the connection members **56.**

3. The package as set forth in claim 2, Corisis et al. show wherein the bonding member (**49, see figure 5**) applied to the first semiconductor chip is a nonconductive bonding agent having spacers therein, the bonding member serving to maintain balance between the first semiconductor chip and the second semiconductor chip and to prevent shorts between the second semiconductor chip and the connection members of the first semiconductor-chip.

5. The package as set forth in claim 1 or 2, Corisis et al. show wherein the connection members **56** are conductive wires.

6. The package as set forth in claim 1, Corisis et al. show wherein the edge-bonding metal patterns (**45, see figure 1**) are connected to the corresponding circuit patterns of

the substrate **52** at the edge regions of the semiconductor chip **20a',20b'** by means of the connection members **56**.

7. The package as set forth in claim 2, Corisis et al. show wherein the edge-bonding metal patterns **(45, see figure 1)** are electrically connected to the corresponding circuit patterns (inherit) of the substrate **52** at the edge regions of the first and second semiconductor chips **20a',20b'** by means of the connection members **56**, respectively.

DOCUMENT-IDENTIFIER: US 2003/0189256 A1

TITLE: Bond pad rerouting element and stacked semiconductor device assemblies including the rerouting element

Summary of Invention Paragraph - BSTX (12):

[0012] Many semiconductor devices include bond pads that are arranged at central locations on an active surface thereof. Examples include semiconductor devices that are configured for use with leads-over-chip (LOC) type lead frames, in which the bond pads are arranged substantially linearly along the centers thereof, as well as semiconductor devices with bond pads disposed in an "I" arrangement. While it may be desirable to use such semiconductor devices in stacked multi-chip modules, the central bond pad placements thereof do not readily facilitate the use of bond wires or other laterally extending discrete conductive elements to electrically connect the bond pads with their corresponding terminal pads of a circuit board that underlies the semiconductor device stack.

Claims 1 to 3 to 5 to 7 are rejected under 35 U.S.C. § 102(e) as being anticipated by Song et al. (U.S. Patent # 6,642,627 B2).

1. Song et al. (figures 1 to 23) specifically figures 11 and 18 show a ball grid array (BGA) package **200** having a semiconductor chip **10,210a,210b** with edge-bonding metal patterns **(15, see figure 11)** formed thereon, comprising: a substrate **(251,see figure 18)** having circuit patterns for electric connection formed therein (inherit); a center-bonding type semiconductor chip **10,210a,210b** attached to the substrate, the semiconductor chip having center-bonding pads **(12, see figure 11)** formed on one side thereof; edge-bonding metal patterns **(15, see figure 11)** electrically connected to the center-bonding pads of the semiconductor chip, the

edge bonding metal patterns being extended towards the edge regions of the center-bonding type semiconductor chip; connection members **(99 in figure 11, 257 in figure 18)** for electrically connecting the edge bonding metal patterns extended towards the edge regions of the semiconductor chip to the circuit patterns of the substrate, respectively; a sealing material **(259,see figure 18)** for molding the substrate to protect the semiconductor chip; and solder balls 271 attached to solder pads **(not shown, but inherit)** electrically connected to the circuit patterns of the substrate, respectively, for transmitting electric signals from the semiconductor chip to an external substrate, wherein the edge-bonding metal patterns **(15, see figure 11)** are in contact with both of the center-bonding pads 12 and the connection members **(see 99 in figure 11)**.

2. Song et al. (figures 1 to 23) specifically figures 11 and 18 show a ball grid array (BGA) package 200 having semiconductor chips **10,210a,210b** with edge-bonding metal patterns **(15, see figure 1)** formed thereon, comprising: a substrate **(251, see figure 18)** having circuit patterns for electric connection formed therein; a first center-bonding type semiconductor chip **(210a, in figure 18)** attached to the substrate, the first semiconductor chip having center bonding pads **(12, see figure 11)** formed on one side thereof; edge-bonding metal patterns **(15, see figure 11)** electrically connected to the center-bonding pads of the first semiconductor chip, the edge-bonding metal patterns being extended towards the edge regions of the first center-bonding type semiconductor chip; a bonding member **(263, see figure 18)** applied to the first semiconductor chip to form a stacked structure; a second center-bonding type semiconductor chip **(210b in figure 18)** stacked on the first semiconductor chip via the bonding member, the second semiconductor chip having center-bonding pads **(12, see figure 11)** formed on one side thereof; edge-bonding metal patterns **(15, see figure 11)** electrically connected to the center-bonding pads of the second semiconductor chip, the edge-bonding metal patterns being extended towards the edge regions of the second center-bonding type semiconductor chip; connection members **(99 in figure 11)** for electrically connecting the edge bonding metal patterns of the first and second semiconductor chips to the circuit patterns

(inherit) of the substrate, respectively; a sealing material (259 I figure 19) for molding the substrate to protect the first and second semiconductor chips; and solder balls 271 attached to solder pads (inherit) electrically connected to the circuit patterns of the substrate, respectively, for transmitting electric signals from the first and second semiconductor chips to an external substrate, wherein the edge-bonding metal patterns (15, see figure 11) are in contact with both of the center-bonding pads 34 and the connection members (99 in figure 11).

3. The package as set forth in claim 2, Song et al. show wherein the bonding member **(263, see figure 18)** applied to the first semiconductor chip is a nonconductive bonding agent having spacers therein, the bonding member serving to maintain balance between the first semiconductor chip and the second semiconductor chip and to prevent shorts between the second semiconductor chip and the connection members of the first semiconductor-chip.

5. The package as set forth in claim 1 or 2, Song et al. show wherein the connection members **(99 in figure 11, 257 in figure 18)** are conductive wires.

6. The package as set forth in claim 1, Song et al. show wherein the edge-bonding metal patterns **(15, see figure 11)** are connected to the corresponding circuit patterns of the substrate **251** at the edge regions of the semiconductor chip **10,210a,210b)** by means of the connection members **99,257**.

7. The package as set forth in claim 2, Song et al. show wherein the edge-bonding metal patterns **(15, see figure 11)** are electrically connected to the corresponding circuit patterns (inherit) of the substrate **251** at the edge regions of the first and second semiconductor chips **210a,210b** by means of the connection members **99,257**, respectively.

DOCUMENT-IDENTIFIER: US 20040041258 A1

TITLE: Semiconductor chip having bond pads and multi-chip package

---------- KWIC ---------

Abstract Paragraph - ABTX (1):

A semiconductor chip comprises a semiconductor substrate having integrated circuits formed on a cell region and a

peripheral circuit region adjacent to each other. A bond pad-wiring pattern is formed on the semiconductor substrate. A pad-rearrangement pattern is electrically connected to the bond pad-wiring pattern. The pad-rearrangement pattern includes a bond pad disposed over at least a part of the cell region. The bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate. Thus, with the embodiments of the present invention, the overall chip size can thereby be substantially reduced and an MCP can be fabricated without the problems mentioned above.

Summary of Invention Paragraph - BSTX (11):

[0011] The ability to reduce the size of a multi-chip package (MCP) including multiple conventional semiconductor chips in a single body package is also limited due to problems such as the difficulty of stacking center pad-type chips on chips of the same or similar types. That is, wire bonding can be complicated and difficult due to long loop wires in such cases.

Summary of Invention Paragraph - BSTX (14):

[0013] A semiconductor chip comprises a semiconductor substrate having integrated circuits formed on a cell region and a peripheral circuit region adjacent to each other. A bond pad-wiring pattern is formed on the semiconductor substrate. A pad-rearrangement pattern is electrically connected to the bond pad-wiring pattern. The pad-rearrangement pattern includes a bond pad disposed over at least a part of the cell region. According to one embodiment, the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate. According to another embodiment, a portion of the pad-rearrangement pattern extends substantially from the center region of the semiconductor substrate toward an edge of the semiconductor substrate. According to yet another embodiment, the bond pad-wiring pattern is form on a portion of the peripheral circuit region and extends across a portion of the cell region.

Brief Description of Drawings Paragraph - DRTX (10):

[0023] FIG. 11 is a cross-sectional view of the semiconductor chip of FIG. 9, following wire bonding;

Detail Description Paragraph - DETX (3):

[0035] The bond pad-wiring pattern 12 is preferably formed in a center region of the semiconductor substrate 11., One end of

the bond pad-wiring pattern 12 is preferably formed on the portion of the peripheral circuit region A.sub.peri. In the conventional semiconductor chip, an additional chip area is needed in peripheral circuit regions for forming bond pads having a minimum size and pitch designed for electric die sorting (EDS) and making electrical interconnections. According to the forgoing embodiment of the present invention, however, no larger additional area for forming bond pads is required, rather only the small portion of the bond pad-wiring pattern 12 needs to be formed on the peripheral circuit region A.sub.peri. The remaining portion of the bond pad-wiring pattern 12 extends across a portion of the cell region according to an embodiment of the present invention. The width of the semiconductor substrate 11 can therefore be reduced by approximately the width of the bond pad area of the conventional semiconductor chip.

Detail Description Paragraph - DETX (6):

[0038] A passivation layer 16 is formed on the bond pad-wiring pattern 12. An interlayer dielectric (ILD) 13 is then formed on the passivation layer 16. The ILD 13 is made of a material having good insulation and integration properties to protect bond pads 17 from mechanical stress due to subsequent wire bonding, beam lead bonding, or ball bonding. For example, a high-density plasma (HDP) oxidized layer, a benzocyclobutene (BCB) layer, a polybenzoxazole (PBO) layer, or a polyimide layer may be used as the ILD 13. An HDP oxide layer using silan, oxygen and argon gases, for example, an HDP-SiO.sub.2 layer is preferably used. The passivation layer 16 and the ILD 13 have openings 14 formed therein to expose predetermined portions of the bond pad-wiring pattern 12a.

Detail Description Paragraph - DETX (9):

[0041] According to one embodiment, the pad-rearrangement pattern 15 reroutes the bond pads 17 from the bond pad-wiring pattern 12 in the peripheral circuit region A.sub.peri to above the cell regions A.sub.cell1 and A.sub.cell2. As shown above, one end of the pad-rearrangement pattern 15 is electrically connected to the exposed bond pad-wiring pattern 12 via openings 14. The other end extends toward the edge of the substrate 11. In other words, according to one aspect of the present invention, the portion of the pad-rearrangement pattern 12 extends substantially from the center region of the semiconductor substrate 11 toward an edge of the semiconductor substrate 11. The bond pads 17 can therefore be formed along sides of the semiconductor substrate 11. Thus, according to

various embodiments of the present invention, peripheral pad type semiconductor chips can be fabricated using center pad type semiconductor chips, which are known to have improved electrical performance characteristics over the peripheral pad type chips. The pitch between the bond pads can increase. During the EDS test, a probe can easily contact the bond pads. These modified peripheral pad chips thus need not be packaged in a lead-on-chip (LOC) type package, but may be implemented in a conventional package.

Detail Description Paragraph - DETX (10):

[0042] Referring to FIG. 11, electrical connection means such as bonding wires 99 are coupled to the bond pads 17. If necessary, the positions of bond pads 17 can be adjusted depending on the design and structure of the electrical interconnections.

Detail Description Paragraph - DETX (14):

[0046] Although the forgoing embodiment comprises a single ILD, the present invention may comprise two or more ILDs, as shown in FIG. 12 and FIG. 17. Referring to FIGS. 12 and 17, second ILDs 20a, 20 can be interposed between the ILD 13 and the pad-rearrangement pattern 15. In particular, as illustrated in FIGS. 12 and 17, because the second ILDs 20a, 20 are interposed between the ILD 13 and the pad-rearrangement pattern 15, the electrical properties of the semiconductor chips 30, 90 are improved. The capacitance, for example, can be lowered. The thickness of the second ILD 20a is between 2 to 50 .mu.m, for example determined base on the capacitance and the intensity supplement. The second ILD 20a may be made of benzocyclobutene (BCB), polybenzoxazole (PBO), polyimide, and so on. Also, in this case, the planarization process is preferably performed on the ILDs to improve the planarity of the ILDs 13, 20a or 20. Accordingly, the planarity of the pad-rearrangement pattern 15 thereon can be in turn improved. Further, connection failures of the bonding wires or the beam leads on the bond pads 17 are prevented and the adhesion therebetween are improved. The planarization is preferably accomplished through chemical and mechanical polishing (CMP).

Detail Description Paragraph - DETX (15):

[0047] According to one aspect of the present invention, the ILDs 13 and 20 of the semiconductor chip 90 (FIG. 17) distribute mechanical stresses during the formation of the electrical interconnections and protect the bond pads 17 from the

mechanical stresses. In addition, since the bond pads 17 are formed after two planarization processes on the two ILDs, the bonding stability of the wire bonding between the bond pads 17 and the external device is improved.

Detail Description Paragraph - DETX (19):

[0051] In particular, Referring to FIGS. 13 through 15, a semiconductor substrate 11 includes a bond pad-wiring pattern 12 preferably formed on at least a portion of the peripheral circuit region A.sub.peri and electrically connected thereto. A passivation layer 16 is formed on the semiconductor substrate 11 and on the bond pad-wiring pattern 12. The first ILD 13 is formed over the semiconductor substrate 11 including the bond pad-wiring pattern 12. A second ILD 20b is then formed over the first ILD 13. A first opening 22 is formed through the first and second ILDs 13, 20b and the passivation layer 16 to expose a portion of the bond pad-wiring pattern 12. A second opening 24 is formed through the second ILD 20b to expose a portion of the first ILD 13. A pad-rearrangement pattern 15 is formed over the second ILD 20b and within the first opening 22 and is electrically connected to the bond pad-wiring pattern 12. The pad-rearrangement patter 15 is also formed within the second opening 24. An insulating layer 18 is formed over the pad-rearrangement pattern 15 and includes an opening 26 therein that exposes a portion of the pad-rearrangement pattern 15 formed within the second opening 24 to define the bond pads 17 over at least a part of the cell region A.sub.cell. The portions of the pad-rearrangement pattern 15 not covered by the insulating layer 18 provide the bond pads 17. This embodiment has the similar features as described previously. For example, the bond pad-wiring pattern 12 is formed substantially in a center region of the semiconductor substrate 11.

Detail Description Paragraph - DETX (20):

[0052] Various MCPs utilizing the semiconductor chips according to the embodiments of the present invention are obtainable, which will be explained below. Referring to FIG. 18, an MCP 200 preferably comprises a first chip 210a and a second chip 210b that are vertically stacked on a package substrate 251. A printed circuit board (PCB) or tape wiring substrate can be used as the package substrate 251. The substrate surface preferably has a plurality of bonding tips 253 formed thereon. The first and second chips 210a and 210b are preferably the same type of chips. The first and second chips 210a and 210b can have structures formed in accordance with the

principles of the present invention described previously. For example, a bond pad-wiring pattern can be formed substantially in a center region of a semiconductor substrate, for example. Accordingly, the bond pads 217a and 217b of the first and second chips 210a and 210b are formed over cell regions along sides of the chips 210a and 210b. Thus, the chips 210a and 210b can have a modified configuration, i.e., a center pad-type chip can be modified into a peripheral pad-typed chip.

Detail Description Paragraph - DETX (21):

[0053] The first and second chips 210a and 210b are electrically connected to the package substrate 251 by electrical connection means such as bonding wires 257, which are in turn electrically connected to the bonding tips 253. Thus, each bonding tip 253 is electrically connected to a corresponding one of the bond pads 271a, 271b.

Detail Description Paragraph - DETX (22):

[0054] The first chip 210a is mounted on the package substrate 251 with an adhesive 261, and the second chip 210b is mounted on the first chip 210a with an adhesive material 263. The adhesive material 263 is interposed between the first and second chips 210a and 210b, thus ensuring enough space for the bonding wires 257 used in connecting the first chip 210a with the package substrate 251.

Detail Description Paragraph - DETX (23):

[0055] An encapsulant 259, formed of a material such as an epoxy molding compound, protects the upper surface of the package substrate 251 from an external environment by encapsulating the first and second chips 210a, 210b and the bonding wires 257. Solder balls 271 are formed on the lower surface of the package substrate 251 to provide external connection terminals.

Detail Description Paragraph - DETX (25):

[0057] Referring to FIG. 19, an MCP 300 according to another embodiment of the present invention comprises a first chip 310a and a second chip 310b mounted side by side on a package substrate 351. Here, the first and second chips 310a, 310b preferably have structures the same as or similar to the structures described in FIG. 21 or the same as or similar to structures of the chip embodiments described above. For example, the first and second chips 310a, 310b are preferably

electrically connected to the substrate 351 by bonding wires 357 through bonding tips 353. Reference numerals 359, 361, 371 are used herein to denote an encapsulant, adhesives, and solder balls, respectively.

Detail Description Paragraph - DETX (27):

[0059] The semiconductor chips 410a, 410b, 410c are preferably electrically connected to the substrate 451 by bonding wires 457 through bonding tips 453. As described above, the MCP 400 of this embodiment can comprise different types of chips. Since the center pad-type chip is modified into a peripheral pad-type chip, it is possible to vertically stack the multiple chips and the lengths of the bonding wires can be made shorter to allow easier wire bonding.

Detail Description Paragraph - DETX (29):

[0061] The MCP 500 of this embodiment does not include die pads for mounting the semiconductor chips 510a, 510b. Instead, the leads of the lead-frame 551 employed in the LOC type package are preferably used. The length of the leads of the lead frame 551 is preferably longer than that of the conventional leads, but this is not required. The upper surface of the first semiconductor chip 510a is attached to lower surfaces of opposing leads of the lead frame 551 by adhesive tape 563. The bond pad 517a of the first chip 510a is disposed between the opposing leads of the lead frame 551 and is wire-bonded to the upper surface of the corresponding leads of the lead frame 551 by bonding wires 557a. The upper surface of the second chip 510b is attached to the lower surface of the first chip 510a with an adhesive 561. The realignment bond pad 517b of the second chip 510b is wire-bonded to the lower surface of the corresponding leads of the lead frame 551 by bonding wires 557b. The first and second chips 510a, 510b and corresponding bonding wires 557a, 557b are encapsulated by an encapsulant 559.

Detail Description Paragraph - DETX (31):

[0063] Referring to FIG. 22, an MCP 600 according to a still further embodiment of the invention is a DDP comprising first and second semiconductor chips 610a, 610b. A die pad 653 and leads 651 are used for mounting the chips 610a, 610b. The first and second chips 610a, 610b are preferably a peripheral pad-type where bond pads 617a, 617b are formed along sides of the chips 610a, 610b. The first and second chips 610a, 610b are attached to the upper and lower surfaces, respectively, of the die pad 653 with an adhesive 661. The bond pads 617a of the first chip

610a are wire-bonded to the upper surfaces of the leads 651 by bonding wires 657a. The bond pads 617b of the second chip 610b are wire-bonded to the lower surfaces of the leads 651 by bonding wires 657b. The first and second chips 610a, 610b and bonding wires 657a, 657b are encapsulated by an encapsulant 659.

Detail Description Paragraph - DETX (35):
[0067] The bond pads 717a, 717b of the first and second chips 710a, 710b are wire-bonded to the upper surface of the lead of the lead frame 751 through first and second bonding wires 757a, 757b, respectively. The bond pads 717c, 717d of the third and fourth chips 710c, 710d are wire-bonded to the lower surface of the lead of the lead frame 751 by third and fourth bonding wires 757c, 757d, respectively. The semiconductor chips 710a, 710b, 710c, 710d and bonding wires 757a, 757b, 757c, 757d are encapsulated with an encapsulant 753. Herein, the reference numerals 761, 762, 763, and 764 each represent an adhesive.

Detail Description Paragraph - DETX (36):
[0068] In various embodiments of the present invention, such as those described previously, electrical connections between the chips and the lead frame or package substrate are preferably made by wire bonding. Other techniques may be used instead, however, to form an MCP according to the present invention.

Initially, and with respect to claim 4, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over in Corisis et al. (U.S. Patent Application Publication # 2003/0189256 A1).

As to the grounds of rejection under section 103, see MPEP § 2113.

Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over in Song et al. (U.S. Patent # 6,642,627 B2).

As to the grounds of rejection under section 103, see MPEP § 2113.

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Corisis et al. (U.S. Patent Application Publication # 2003/0189256 A1) in view of Miyagawa (U.S. Patent # 6,780,023).

Corisis et al. show the features of the claimed invention as detailed above, but fail to explicitly show wherein the sealing material is synthetic resin.

Miyagawa is cited for showing printed circuit board having plurality of conductive patterns passing through adjacent pads. Specifically, Miyagawa (figures 1 to 6) specifically figure 6 discloses wherein the sealing material **17** is synthetic resin for the purpose of protecting a printed circuit board surface which permits passing a plurality of conductive patterns between adjacent pads without complicating the pad shape and layout.

(3) FIG. 1 shows a circuit module 11 used in an electric apparatus such as a portable computer. The circuit module 11 comprises a ball grid array (BGA) type semiconductor package 12 and a printed wiring board 13.
(4) The semiconductor package 12 constitutes a surface mount circuit component. The semiconductor package 12 comprises a package substrate 14, an IC chip 15 and a plurality of solder balls 16. The package substrate 14 has a first surface 14a and a second surface 14b as a terminal surface. The second surface 14b is the opposite side of the first surface 14a. The IC chip 15 is mounted on the first surface 14a of the package substrate 14, and is covered by a synthetic resin mold material 17.

Therefore, it would have been obvious to one of ordinary skill in the art to use Miyagawa's synthetic resin to modify Corisis et al.'s sealing material for the purpose of protecting a printed circuit board surface which permits passing a plurality of conductive patterns between adjacent pads without complicating the pad shape and layout.

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Song et al. (U.S. Patent # 6,642,627 B2) in view of Miyagawa (U.S. Patent # 6,780,023).

Song et al. show the features of the claimed invention as detailed above, but fail to explicitly show wherein the sealing material is synthetic resin.

Miyagawa is cited for showing printed circuit board having plurality of conductive patterns passing through adjacent pads. Specifically, Miyagawa (figures 1 to 6) specifically figure 6 discloses wherein the sealing material **17** is synthetic resin for the purpose of protecting a printed circuit board surface which permits passing a plurality of conductive patterns between adjacent pads without complicating the pad shape and layout.

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Therefore, it would have been obvious to one of ordinary skill in the art to use Miyagawa's synthetic resin to modify Song et al.'s sealing material for the purpose of protecting a printed circuit board surface which permits passing a plurality of conductive patterns between adjacent pads without complicating the pad shape and layout.

Response

Applicant's arguments filed 2/2/05 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claims 1 and 2" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. ∋ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. ∋ 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. ∋ 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/777,686,723,685,200,698,696,690,691	11/6/04 4/10/05
Other Documentation: foreign patents and literature in 257/777,686,723,685,200,698,696,690,691	11/6/04 4/10/05
Electronic data base(s): U.S. Patents EAST	11/6/04 4/10/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
4/10/05